REMARKS

Favorable reconsideration and allowance of the claims of the present application are respectfully requested.

Before addressing the specific grounds of rejection raised in the present Office Action, applicants have made amendments to independent Claims 12 and 28. Specifically, applicants have amended both Claims 12 and 28 to positively recite that a single asymmetric FET device is located on an upper surface of an insulator. Support for this amendment to Claims 12 and 28 is found in the various drawings of the present application. See, for example, FIG. 7B. Note in FIG. 7B, 12 denotes the vertical semiconductor body, 26 represents a gate portion (n or p) and 24 represents another gate portion (n or p) that has an opposite conductivity than gate portion 26. In the drawing, reference numeral 16 denotes the gate oxide that separates the vertical semiconductor 12 from the gate portions 24 and 26, respectively. Hence, the illustrated structure includes a single asymmetric FET device.

Applicants have also amended Claims 12 and 28 to positively recite that a double doped region 28 is located adjacent to gate portions 26 and 24, respectively. See FIG. 7, for example, and Page 7, lines 23-28.

Applicants respectfully submit that the above amendments to Claims 12 and 28 were performed to more precisely claim the present invention described and illustrated in the present application. Since the above amendments to the claims do not introduce new matter to the application, entry thereof is respectfully requested.

Claims 12, 20-22, and 24-27 stand rejected under 35 U.S.C. § 102(e) as allegedly anticipated by U.S. Patent No. 6,503,784 to Enders, et al. ("Enders, et al."). Claims 14-18 and 28 stand rejected under 35 U.S.C. § 103 as allegedly unpatentable over the disclosures of Enders, et al and U.S. Patent No. 5,872,045 to Lou, et al. ("Lou, et al.").

With respect to the § 102(e) rejection, it is axiomatic that anticipation under § 102 requires that the prior art reference disclose each and every element of the claim to which it is applied. In re King, 801 F.2d 1324, 1326, 231 U.S.P.Q. 136, 138 (Fed. Cir. 1986). Thus, there must be no differences between the subject matter of the claim and the disclosure of the applied prior art reference. Stated another way, the reference must contain within its four corners adequate direction to practice the invention as claimed. The corollary of the rule is equally applicable: The absence from the applied reference of any claimed element negates anticipation. Kloster Speedsteel AB v. Crucible Inc., 793 F.2d 1565, 1571, 230 U.S.P.Q. 81, 84 (Fed. Cir. 1986).

Applicants respectfully submit that Claims 12, 20-22, and 24-27 of the present application are not anticipated by the disclosure of Enders, et al. since the applied reference does not teach applicants' claimed structure recited in amended Claim 12. Specifically, Enders, et al. do not disclose an asymmetric FET which includes, among other features, *a single asymmetric FET device located on an upper surface of an insulator*. Moreover, Enders, et al. do not disclose the presence of a *double doped region adjacent to each gate portion of the single asymmetric FET device*, as is presently recited in the claimed structure.

Enders, et al. disclose a structure that includes a pair of vertical double gate devices. See, Col. 8, lines 23-24 of the prior art. The applied reference does not disclose, however, a single asymmetric FET device, as presently claimed. Applicants observe that in the structure disclosed in Enders, et al., none of the components thereof is a double doped region, let alone a double doped region that is located adjacent to each gate portion of a single asymmetric FET device.

The foregoing remarks clearly indicate that the applied reference does not teach each and every aspect of the claimed invention as required by King and Kloster Speedsteel; therefore the claims of the present application are not anticipated by the disclosure of Enders, et al.

Turning to the § 103 rejection, applicants respectfully submit that the claims of the present application are not made obvious from the combined disclosures of Enders, et al. and Lou, et al. since the applied references do not teach or suggest applicants' asymmetric FET which includes a single asymmetric FET device that is located on an upper surface of an insulator and a double doped region adjacent to each gate portion of the single asymmetric FET. Specifically, Enders, et al. are defective for the various reasons mentioned above. Enders, et al. do not teach or suggest applicants' claimed structure recited in amended Claim 12 or amended Claim 28. Specifically, Enders, et al. do not teach or suggest an asymmetric FET which includes, among other features, *a single asymmetric FET device located on an upper surface of an insulator.* Moreover, Enders, et al. does not disclose the presence of a *double doped region adjacent to each gate portion of the single asymmetric FET device*, as is presently recited in the claimed structure.

In contrast, Enders, et al. disclose a structure including a pair of vertical double-gated transistors, not a single asymmetric FET, as presently claimed. Moreover, the prior art structure does not contain a double doped region therein, let alone a double doped region that is adjacent to each gate portion of a single asymmetric FET device. As such, Enders, et al. do not teach or suggest applicants' claimed asymmetric FET recited in the claims of the present application.

Lou, et al. do not alleviate the above defects in Enders, et al. since the applied secondary reference also does not teach or suggest applicants' claimed structure that includes *a single asymmetric FET device located on an upper surface of an insulator*. Moreover, Lou, et al. do not disclose the presence of a *double doped region adjacent to each gate portion of the single asymmetric FET device*, as is presently recited in the claimed structure.

Applicants observe that Lou, et al. disclose a method for making an improved global planarized surface that includes SiO_2 or undoped polySi for the planarized surface. The applied secondary reference does not disclose an asymmetric FET device, let alone the structure presently recited in the claims of the present application.

The § 103 rejection also fails because there is no motivation in the prior art references that suggests modifying the prior art structures to arrive at applicants' claimed asymmetric FET, which includes the various features recited in amended Claims 12 and 28. The § 103 rejection is thus improper since the prior art does not suggest this drastic modification, which is required in the claims of the present application.

The law requires that the prior art reference provide some teaching, suggestion or motivation to make the modification. Here, there is no motivation provided in the disclosures of Enders, et al. and/or Lou, et al. which would lead one skilled in the art to form the claimed structure. "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." In re Fritch, 972 F.2d 1260, 1266, 23 U.S.P.Q. F.2d 1780, 1783-84 (Fed. Cir. 1992). There is no suggestion in the prior art to modify the semiconductor structures to one having applicant's claimed features. As such, the claims of the instant application are not obvious from the disclosures of Enders, et al and Lou, et al.

Based on the above amendments and remarks, the rejection to the claims under 35 U.S.C. § 103 has been obviated; therefore reconsideration and withdrawal of the instant rejections are respectfully requested.

Wherefore, reconsideration and allowance of the claims of the present application, as amended herein, are respectfully requested.

Respectfully submitted,

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